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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,466	04/08/2004	Zunghang Yu	A1168	1091

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EXAMINER	
MEMULA, SURESH	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/821,466	YU ET AL.
	Examiner	Art Unit
	Suresh Memula	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 10-16* is/are rejected.

7)☒ Claim(s) *3-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Paul Dinh

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 12 is objected to under 37 CFR 1.75(c), as being of improper dependent form for claiming dependency to itself. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 12 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter, "nonprogrammable", which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 12, and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation "the programmable portion" in lines 16-17. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "the other electronic device" in lines 12-13. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 14, the phrase "etc." renders the claim indefinite because the claim includes elements not actually disclosed (i.e., those encompassed by "or the like", "such as", and "ect"), thereby rendering the scope of the claim unascertainable. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, and 10-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Tochio el al. (US Patent No. 5,911,061).

As to Claim 1,

partitioning the PLD chip (Column 1, lines 36-37, Column 2, lines 11-13) into a plurality of blocks (Abstract, Column 4, lines 29-31, and FIG 11, FIG.17);

generating a block level RTL model of one of the plurality of blocks (Column 2, lines 10-13, and FIG. 2, and 17);

generating a block level functional representation of the one of the plurality of blocks (Abstract, and FIG. 4-5, and 8);

producing a full chip RTL model using the block level RTL model and the block level functional representation (FIG. 13 and 17); and

using the full chip RTL model for verification, simulation or debugging (Abstract, Column 4, line 25, Column 4, lines 37-39, and FIG. 12-13, 17).

As to Claim 10, the PLD is a complex programmable logic device ("CPLD"), programmable array logic ("PAL"), programmable logic arrays ("PLA"), field PLA ("FPLA"), erasable PLDS ("EPLD"), electrically erasable PLD ("EEPLD"), logic cell arrays ("LCA") or field programmable gate arrays ("FPGA") (Abstract, and Column 1, lines 36-37).

As to Claim 11, the programmable logic device is embedded into another programmable logic device electronic device (Column 2, lines 41-42, and FIG. 16).

As to Claim 14, one or more of the plurality of blocks are digital signal processing blocks, input/output blocks, memory blocks, etc (FIG. 1).

As to Claim 15, a data processing system for verifying a full-chip electronic design of a programmable logic device (PLD) chip (Abstract, Column 4, line 25, Column 4, lines 37-39, and FIG. 12-13, 17), the data processing system including instructions for implementing the method of claim 1 (FIG 12A).

As to Claim 16,

partitioning the programmable region into a plurality of blocks (Abstract, Column 4, lines 29-31, and FIG. 2, 8-9, and 17);

generating a block level RTL model of one of the plurality of blocks (FIG. 2, 12, and 17);

generating a block level functional representation of the one of the plurality of blocks (FIG. 2, 4-5 and 17);

producing a full region RTL model from the block level RTL model and the block level functional representation (FIG. 13, and 17); and

using the full region RTL model for verification, simulation or debugging (FIG. 12A, 13, and 17).

2. Claims 1-2, and 10-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin el al. (US Patent No. 6,651,225).

As to Claim 1,

partitioning the PLD chip (Column 82, lines 36-37) into a plurality of blocks (FIG. 8,13-14, 21, 23, and 39);

generating a block level RTL model of one of the plurality of blocks (Column 15, lines 64-65, Column 16, lines 1-7, and FIG. 4, and 6);

generating a block level functional representation of the one of the plurality of blocks (FIG. 7-8, 23-24, and 27);

producing a full chip RTL model using the block level RTL model and the block level functional representation (FIG. 27, 29, 44, 89); and

using the full chip RTL model for verification, simulation or debugging (Column 16, lines 11-16, Column 17, lines 17-20, and FIG. 2-6, 16, and 25).

As to Claim 2, the programmable portion is partitioned into a plurality of rows and columns of logic array blocks (LABs) (Column 66, lines 57-61, and 66-67).

As to Claim 10, the PLD is a complex programmable logic device ("CPLD"), programmable array logic ("PAL"), programmable logic arrays ("PLA"), field PLA ("FPLA"), erasable PLDS ("EPLD"), electrically erasable PLD ("EEPLD"), logic cell arrays ("LCA")) or field programmable gate arrays ("FPGA") (Abstract, and Column 82, lines 36-37).

As to Claim 11, the programmable logic device is embedded into another programmable logic device electronic device (Column 17, lines 13-16).

As to Claim 12, the other electronic device comprises programmable (Abstract, and FIG. 5 and 8) and non-programmable circuitry (Column 69, line 28, Column 93, line 29, Column 97, lines 19-21, and FIG. 9).

As to Claim 13, the LAB comprises a plurality of one or more of the following sub-blocks: LE, LIM, LAB wide, LEIM, CRAM and DIM (Column 43, lines 38-39, Column 66, line 54, Column 66, line 66, and Column 91, line 39).

As to Claim 14, one or more of the plurality of blocks are digital signal processing blocks, input/output blocks, memory blocks, etc (Column 66, lines 60-63).

As to Claim 15, a data processing system for verifying a full-chip electronic design of a programmable logic device (PLD) chip, the data processing 'system including instructions for implementing the method of claim 1 (FIG. 26 and 28).

As to Claim 16,

partitioning the programmable region (Column 16, lines 1-7) into a plurality of blocks (FIG. 8,13-14, 21, 23, and 39);

generating a block level RTL model of one of the plurality of blocks (Column 15, lines 64-65, Column 16, lines 1-7, and FIG. 4, and 6);

generating a block level functional representation of the one of the plurality of blocks (FIG. 7-8, 23-24, and 27);

producing a full region RTL model using the block level RTL model and the block level functional representation (FIG. 27, 29, 44, and 89); and

using the full region RTL model for verification, simulation or debugging (Column 16, lines 11-16, Column 17, lines 17-20, and FIG. 2-6, 16, and 25).

3. Claims 1, and 10-11, and 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Bajuk el al. (US Patent Pub. 2004/0268288).

As to Claim 1,

partitioning the PLD chip into a plurality of blocks (Paragraph 0002, and FIG. 1b, 1c, and 2);

generating a block level RTL model of one of the plurality of blocks (Abstract, Paragraph 0004, and FIG. 1a and 6);

generating a block level functional representation of the one of the plurality of blocks (FIG. 3);

producing a full chip RTL model using the block level RTL model and the block level functional representation (Paragraph 0006, and FIG. 6); and

using the full chip RTL model for verification, simulation or debugging (FIG. 6).

As to Claim 10, the PLD is a complex programmable logic device ("CPLD"), programmable array logic ("PAL"), programmable logic arrays ("PLA"), field PLA ("FPLA"), erasable PLDS ("EPLD"), electrically erasable PLD ("EEPLD"), logic cell arrays ("LCA") or field programmable gate arrays ("FPGA") (Title, Abstract, Paragraph 0002).

As to Claim 11, the programmable logic device is embedded into another programmable logic device electronic device ().

As to Claim 12, the other electronic device comprises programmable and non-programmable circuitry (Paragraph 0006).

As to Claim 15, a data processing system for verifying a full-chip electronic design of a programmable logic device (PLD) chip, the data processing 'system including instructions for implementing the method of claim 1 (FIG. 4a, 4b, and 4c).

Allowable Subject Matter

Claims 3-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-9 would be allowable because the prior art of record does not teach or suggest the following limitations:

(In Claim 3) creating a block level schematic of an electronic design; extracting a block Ram Bit Address (RBA) file from the block level schematic; extracting a block level

CRAM array from the block level RBA file; and generating the block level RTL using the block level CRAM array.

In Claim 6, creating a block level schematic of an electronic design; generating a full chip schematic using a plurality of the block level schematics; producing a full chip RBA file from the full chip schematic; extracting block level RBA file from the full chip RBA file; extracting a block level CRAM array from the block level RBA file; and generating a block level RTL model using the block level CRAM array.

In Claim 9 comparing the block level RTL model to the block level schematic before producing a full chip RTL model; and modifying the block level functional representation and the block level CRAM array if the block level RTL is not equivalent to the block level schematic.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh Memula whose telephone number is (571) 272-8046. The examiner can normally be reached on M-F 8am-4:30pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SM 3/3/2006

Paul Dinh

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